SLM Process, Voltage and Temperature (PVT) Monitor IP

Highlights

- Modular solution
- High accuracy monitoring
- Digital interfaces for each PVT monitor
- Configurable by customer application

Target Applications

- Data Center, AI, Automotive, 5G and IoT and Consumer Electronics
- Advanced node (FinFET, GAA) semiconductor devices
- Lifecycle management and design enhancement

Technology

- PVT Monitor IP with PVT controller
- Standard digital interfacing
- Advanced node and FinFET SoCs
- 28nm down to 2nm

Overview

Driven by the demand for ever-increasing design complexity and device gate density, the adoption of Process, Voltage and Temperature (PVT) monitoring is critical to achieve reliable operation and optimum performance of advanced node (FinFET, Gate-All-Around (GAA)) semiconductor devices. Increasing transistor density, multi-die ICs and pushing silicon performance boundaries is making monitoring of PVT parameters throughout the silicon lifecycle a necessity. Based on the output of these monitors actions can be taken to optimize silicon health.

The Synopsys SLM PVT IP portfolio includes process detector, voltage monitor, glitch detector, power on reset/brown out reset, temperature sensor, distributed temperature sensor, catastrophic temperature sensor and thermal diode. The monitors are available from 28nm down to 2nm (Including N3E, N3P, N3AE, Intel 18A, N4P, N5, N5A, N6, N7, N7Auto, 12FFC/FFCP and 16FFC). The IP allows for life-cycle analytics, increased performance optimization and enhanced reliability for applications such as data center, AI, automotive, 5G and consumer in both commercial and automotive grade.

For GAA process nodes the monitors will leverage digitally assisted analog (DAA) architecture providing smaller size and ease of integration.

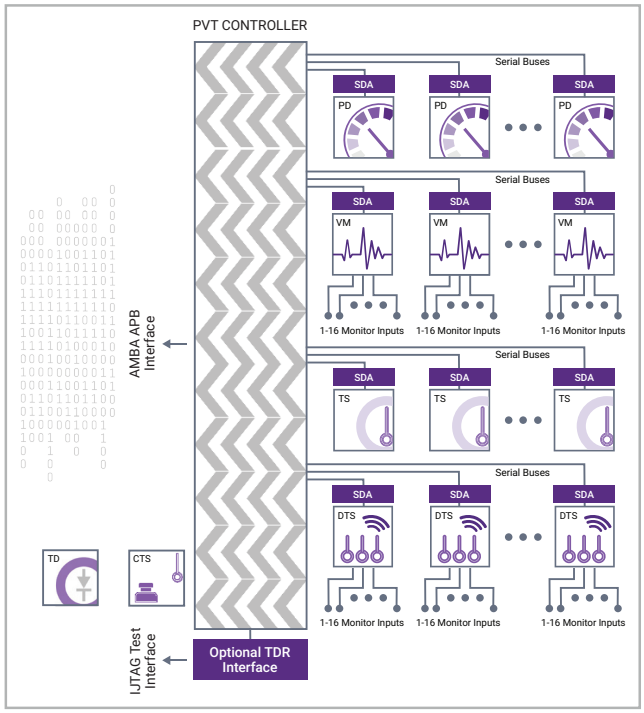

Figure 1: PVT Controller with SLM PVT Monitor IP

Unique Modular Solution

Once integrated, the SLM PVT Monitor IP provides visibility of process, supply and thermal conditions that are accessible via standard interfaces. Through chip assessment and by accurately measuring dynamically changing conditions, the SLM PVT Monitor IP will support device screening and power/performance optimization schemes. The localized, low latency monitoring solution enables an enhanced opportunity for power reduction, increased data throughput and extended device lifetime at both chip and system level. Features include:

- Real-time thermal mapping across the die
- Localized supply voltage analysis
- Silicon assessment for enhanced device screening and increased performance
- Energy and power optimization scheme support (DVFS, AVS)
- Extended reliability and support for predictive maintenance and failure

SLM PVT Monitors

Easy to integrate, the embedded monitoring subsystem includes the following key components:

Process Detector (PD) - Assessment of silicon for device screening, age monitoring and tracking of real-time circuit speed performance.

Voltage Monitor (VM) - High accuracy supply measurement and IR drop analysis during bring-up, production test and in-field device operation.

Temperature Sensor (TS and DTS) - Distributed, low-latency thermal mapping across the die allowing for real-time analysis device activity.

Glitch Detector (GD) - Detect voltage glitches above or below an average voltage level as configured.

*Power on Reset/Brown out Reset (POR/BOR) - Holds reset logic level for a pre-determined time till supplies are stable. BOR issues a reset signal if voltage falls below reliable operating level.

Catastrophic Temperature Sensor (CTS) - Monitors and provides alert on thermal runaway

Thermal Diode (TD) - Monitors die temperature using external current source
**Under Development*

PVT Controller and Driver

The comprehensive solution consists of a range of monitors communicating to a PVT Controller. Configurable by application, the PVT controller is easily integrated into the design-flow and architecture of the chip.

As a major contributor to the Silicon Lifecycle Management Family platform, the flexible solution accommodates the evolving landscape of PVT monitoring and analytics solutions designed to measure in-chip conditions continuously throughout a silicon chip's lifetime, from fabrication to end-of-life. The PVT controller features include:

- Standard interfacing, including AMBA APB and iJTAG test access support
- Flexible configuration when implementing the SMH and register map
- Supports of multiple monitor IP instances
- Auto-polling and configurable monitor duty cycling
- Low system overhead, relieves system control of monitor management tasks
- Alerts, alarms and trigger conditions for safer, more reliable chip operation

A reference bare metal software driver is now also included with the PVT Controller Series 5 that is ISA (Instruction Set Architecture) agnostic and portable.

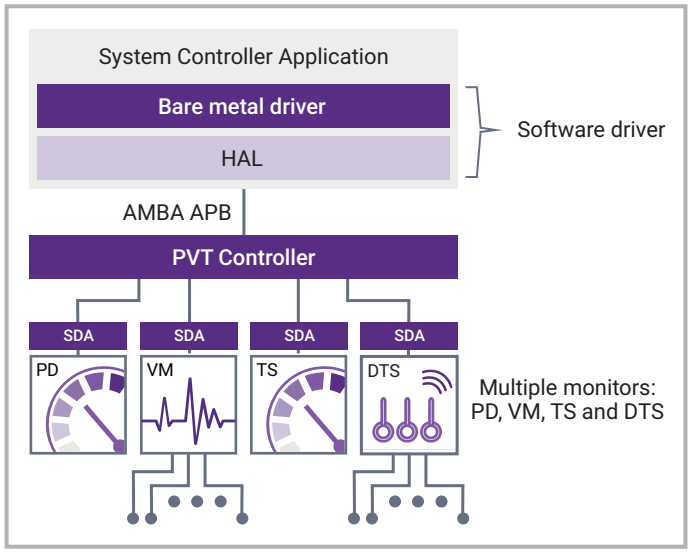

Figure 2: Reference bare metal software driver

Enabling SLM with PVT Monitors

The Synopsys SLM family is designed to improve silicon health and operational metrics at every phase of the device lifecycle. SLM is built on a foundation of PVT monitor IP, data analytics and design automation. Environmental, structural and functional monitors enable deep insights from SoC manufacturing to in-field systems. Meaningful data is gathered at every opportunity for continuous analysis and actionable feedback.

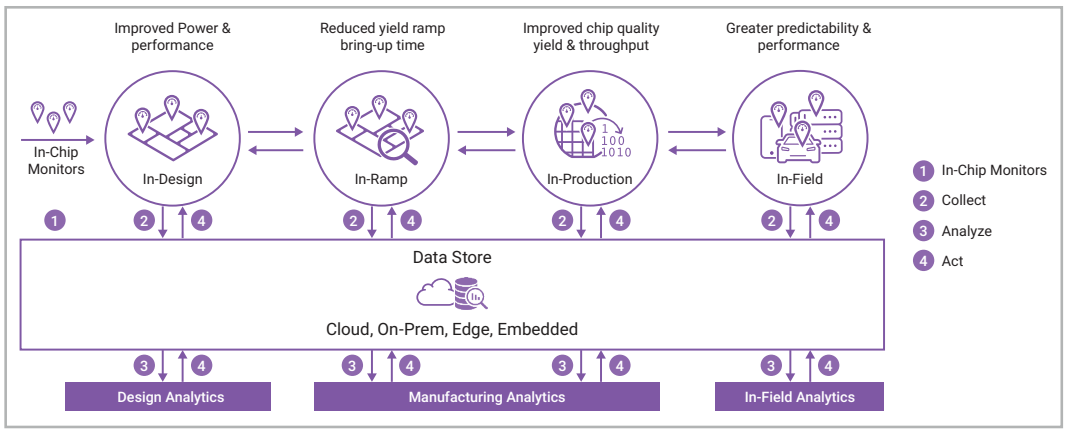

Figure 3: The Synopsys SLM Family is built on a foundation of PVT monitor IP, data analytics and design automation

Key Features:

- Modular solution
- High accuracy monitoring
- Digital interfaces for each PVT monitor
- Configurable by customer application

Key Benefits:

- Understanding process gradient across the die
- Supply voltage tracking and IR drop analysis
- Provides highly granular thermal mapping across the die

Silicon Assessment and Health Monitoring

- Provides real-time adaptive adjustments of test limits versus the traditional DPAT approach, improving quality as measured by DPPM as well as yield
- Correlation of monitor data with existing parametric test data providing real-time accurate, adaptive adjustment of the upper and lower limits on a per die basis
- Process spread measurement during test phase
- Per-chip optimization for power and speed performance
- Age monitoring of silicon during device lifecycle
- Predictive reliability for extended SoC lifetime

Deliverables

A comprehensive set of front-end and back-views are delivered to ensure ease of integration.

Documentation

- Databooks, Application Notes and Silicon reports (subject to availability)

Front End (FE) Views

- LEF
- Verilog Model
- Single Liberty timing file for evaluation purposes only
- Readme

Back End (BE) Views

- GDS Collateral (including tag and layer summary)
- DFT
- DRC Report (including antenna report)
- LVS Report (including ERC report)
- CDL Netlist (for LVS purposes only
- Full Set of Liberty timing files
- CTL file for scan chain stitching
- CSV files – containing ring frequency data
- Verilog gate level netlist for pattern generation (ATPG)

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries , embedded memories, analog IP , wired and wireless interface IP , security IP , embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip .

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